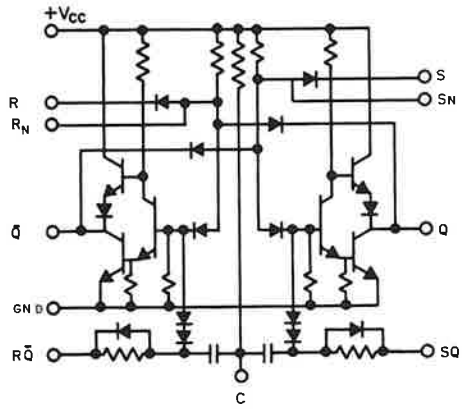
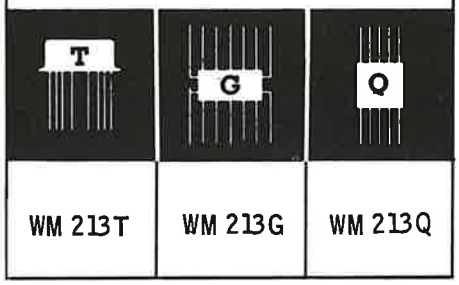
silicon planar epitaxial monolithic integrated circuit for digital systems



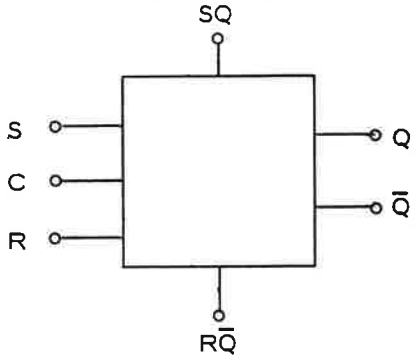

**packages and type numbers**




| WM 213T | WM 213G | WM 213Q |
|---|---|---|

The Westinghouse PULSE BINARY consists of a bistable circuit capable of driving large capacitance loads, with a steering network for trigger action. It can be connected for binary counter or shift register operation. The counting rate is typically 11 mega-cycles.

**logic symbol**




**design features**①

- *11 MC clock rate*
- *full MIL temperature range*
- *fan out 8 over temperature*
- *only one power supply required*
- *3 packages available:*
  *T style modified TO-5*
  *G style 1/4" x 1/8" FLAT-PAK*
  *Q style 1/4" x 1/4" FLAT-PAK*

**reliability assurance**

EVERY unit receives

- high temperature storage bake at +150°C
- 3 cycles of thermal shock −55°C to +150°C
- 20,000 G centrifuge
- gross and helium hermeticity tests

① at $V_{cc}$ = 6.0V at 25°C

**truth table**

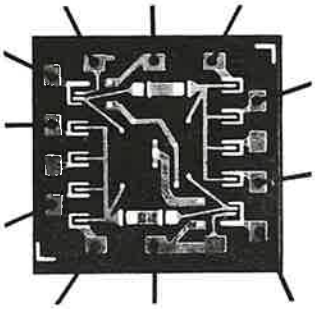
| CLOCKED SET-RESET | | | DIRECT SET-RESET | | |
|---|---|---|---|---|---|
| SQ | RQ̄ | $Q_{(n+1)}$ | S | R | $Q_n$ |
| 0 | 0 | ** | 0 | 0 | * |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | $Q_n$ | 1 | 1 | $Q_n$ |

Logic Definition: 1 − State ~ 2V
0 ÷ State ~ 0.3V

* Both Outputs in 1 − State

** Indeterminate

## electrical characteristics



typical planar, epitaxial silicon integrated circuit

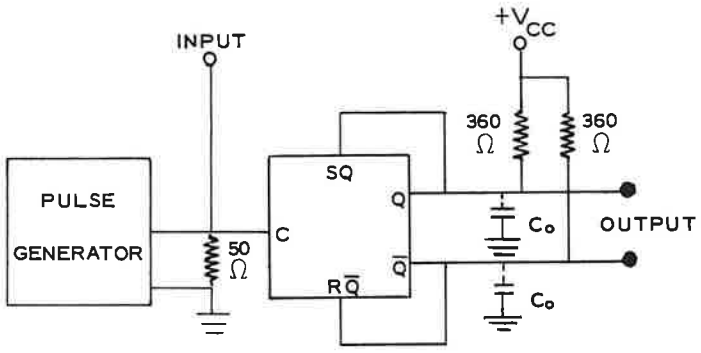
## absolute maximum ratings①

| parameter | symbol | value | units |
|---|---|---|---|
| supply voltage. . . . . | $V_{cc}$ | +8 | volts |
| input voltage. . . . . | $V_{in}$ | +8② | volts |
| node voltage. . . . . | $V_n$ | +8 | volts |
| output voltage . . . . . | $V_{out}$ | +7② | volts |
| ambient storage temperature . . . | $T_{stg}$ | -65 to +175 | °C |
| ambient operating temperature. . | $T_{opg}$ | -55 to +125 | °C |

| Parameter | Symbol | Limit | Values at Temperature −55°C | Values at Temperature +25°C | Values at Temperature +125°C | Units |
|---|---|---|---|---|---|---|
| **static electrical characteristics for $V_{cc}$ = +6.0 volts** | | | | | | |
| total power consumption for symetrical clock input | $P_T$ | max | 55 | 50 | 45 | mw |
| | | typ | | 35 | | mw |
| DC set and reset input current | $I_S$, $I_R$ | max | 2.1 | 1.8 | 1.5 | ma |
| DC node current | $I_{SN}$, $I_{RN}$ | max | 2.5 | 2.1 | 1.8 | ma |
| input reverse current | $I_R$ | max | | 2 | | μa |
| $I_{OUT}$ at $V_{CE(SAT)}$ | $I_{OUT}$ | min | 20 | 16.5 | 9 12 | ma |
| | $V_{CE(SAT)}$ | max | .55 | .45 | .35 .40 | volts |
| fan out available | $F_O$ | min | 9 | 9 | 6 8 | |
| D.C. clock input current | $I_{CL}$ | max | | 3.5 | | ma |
| Output voltage (1-state), 1.8KΩ output to ground | $V_{OFF}$ | min | 3.0 | 3.5 | 3.8 | volts |
| **dynamic electrical characteristics for $V_{cc}$ = +6.0 volts** | | | | | | |
| switching time (see figure 1) | | | | | | |
| turn-on time | $T_{on}$ | max | | 70 | | ns |
| turn-off time | $T_{off}$ | max | | 50 | | ns |
| Least triggering amplitude $t_f$ = 50 ns, 100 ns wide pulse | | typ | 2.4 | 1.9 | 1.6 | volts |
| counting rate (35 ns pulse width) | | typ | | 12 | | Mc |
| | | min | | 10 | | |

① Limiting values beyond which the serviceability of the device may be impaired.

② These terminals must not be biased negatively with respect to ground.



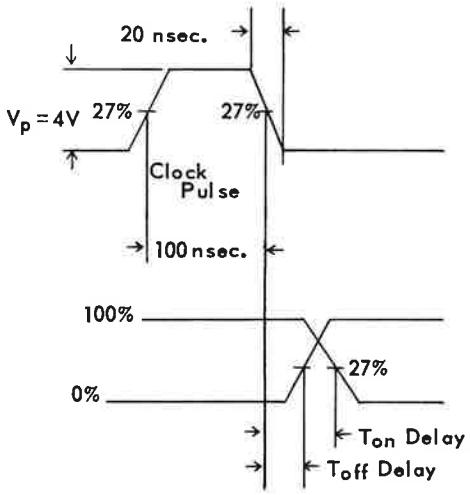




figure 1

## typical electrical characteristics

$V_{in}$ vs. $V_{out}$

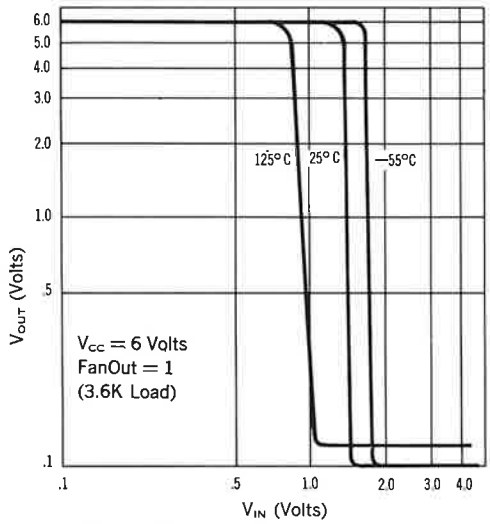



figure 2

$V_{in}$ vs. $V_{out}$

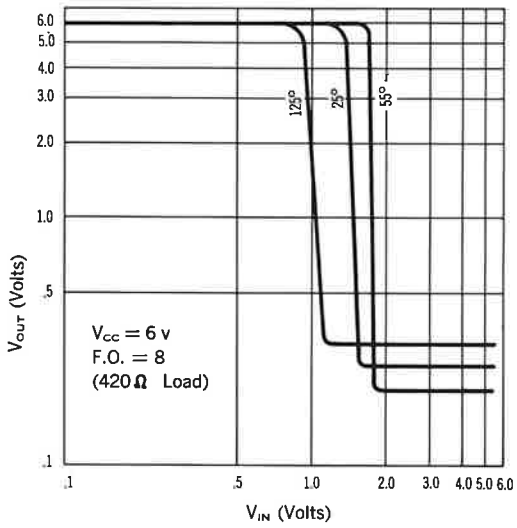



figure 3

output current vs. temperature

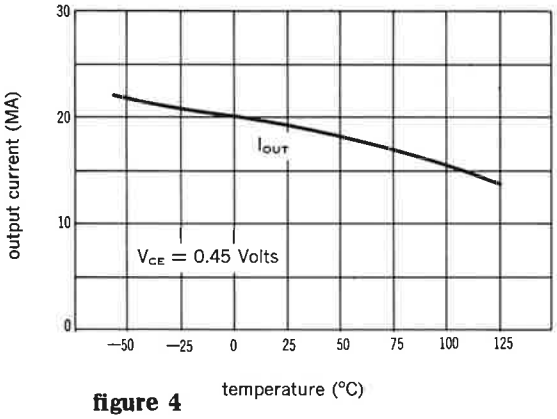



figure 4

input current vs. temperature

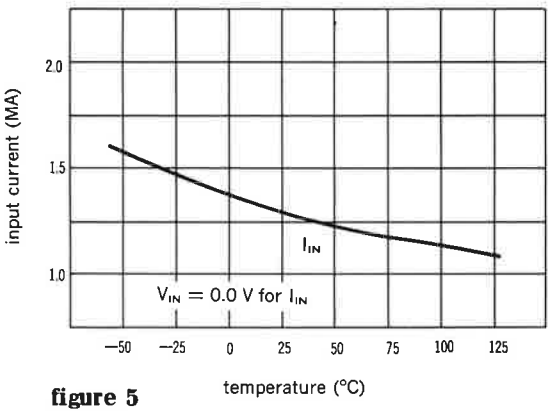



figure 5

power consumption for symetrical clock input

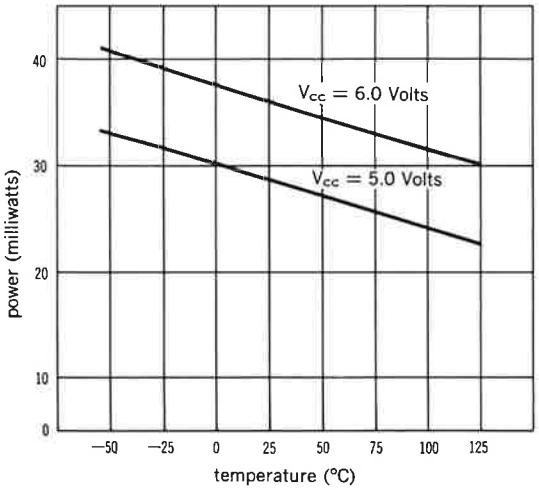



figure 6

output current vs. saturation voltage

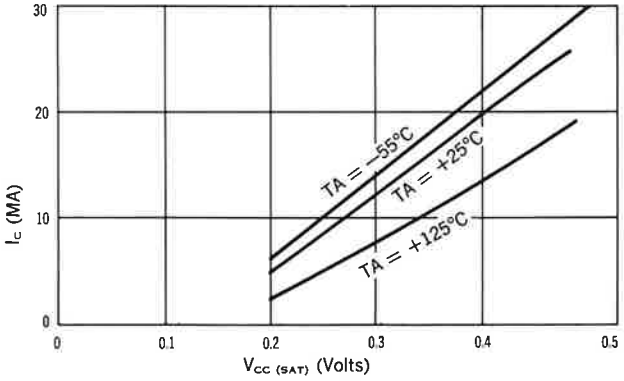



figure 7

## typical electrical characteristics

maximum clock frequency vs. temperature

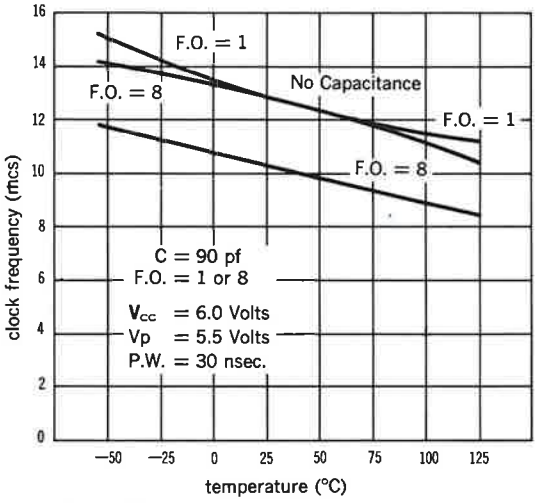



figure 8

$T_{on}$ and $T_{off}$ delay vs. temperature

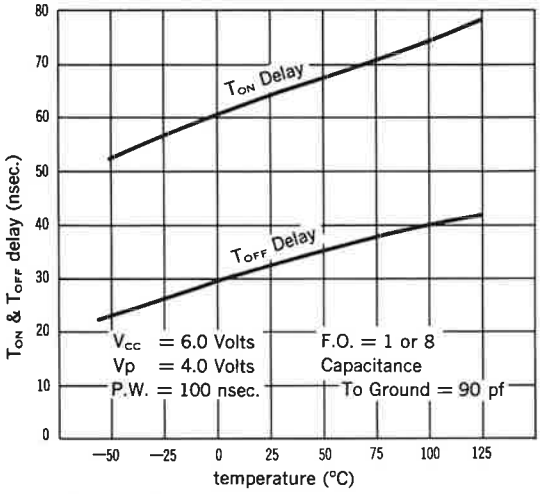



figure 10

$T_{on}$ delay vs. output capacitance to ground

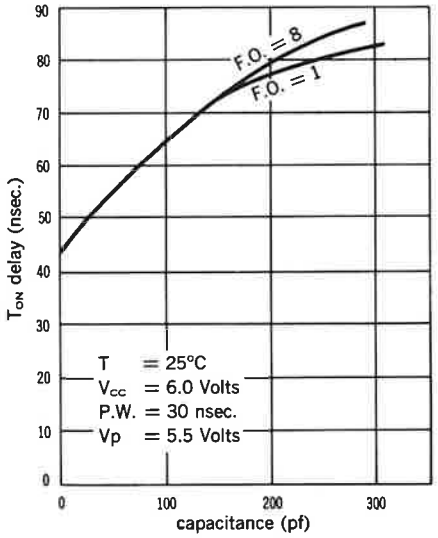



figure 12

maximum operating frequency vs. output capacitance to ground

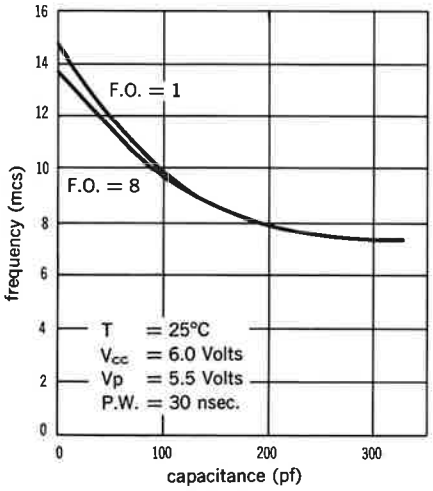



figure 9

typical clock pulse requirements for WM 213

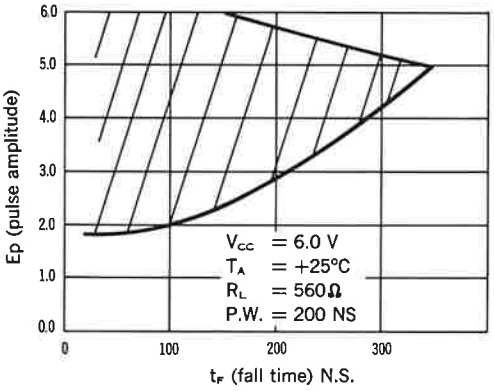



figure 11

$T_{off}$ delay vs. output capacitance to ground

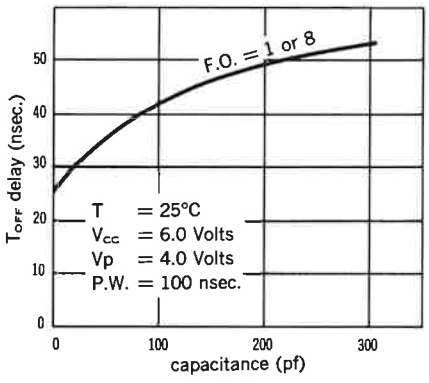



figure 13

## design and application data

The clock pulse recommended is a positive going pulse of 4 volts amplitude, 40 ns width, with a fall time of between 20 and 120 ns. The flip-flop will change state on the negative going edge of the clock pulse, if the correct levels on the clocked set and reset inputs are applied.

The WM 213 may be used as a binary counter element, a shift register element, a clocked RS flip-flop, or a direct RS flip-flop. When used as a binary counter element, the clocked set SQ should be connected to Q, and the clocked reset $R\overline{Q}$ should be connected $\overline{Q}$. Thus on each negative going clock pulse the output of the WM 213 will change state.

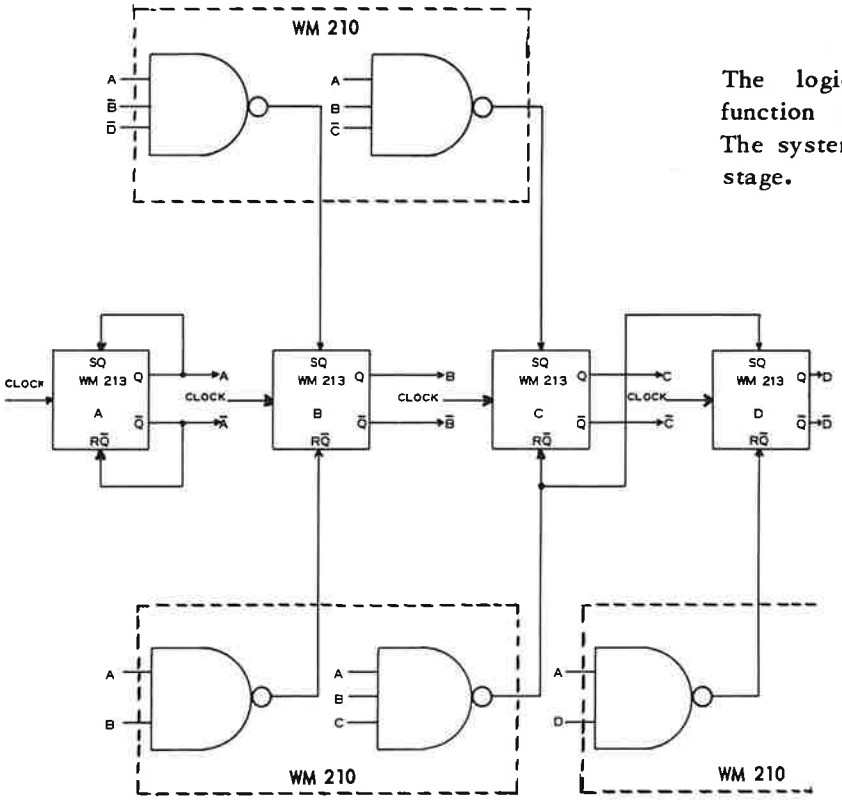
For a shift register stage, SQ should be connected to the complementary output of the preceding bit, and $R\overline{Q}$ should be connected to the true output of the preceding bit. The information in the preceding bit will be transferred forward when the negative edge of the clock pulse occurs.

As a clocked RS flip-flop, the appropriate gating should be applied to the inputs SQ and $R\overline{Q}$ to force the flip-flop to change states according to the logic of the system. A 0–state is an enable for the clock to change the state of the flip-flop. Note that SQ and $R\overline{Q}$ should never be in the 0–state at the same time because the state of the flip-flop after clocking will be indeterminate.

In using the WM 213 for these applications, the direct set and reset inputs S and R should be open or have a 1–state input. If either S or R is in the 0–state, it unconditionally controls the output of the flip-flop.

For a direct RS flip-flop the diodes will be the controlling inputs. Thus SQ and $R\overline{Q}$ should be in the 1–state or open circuited, or there should be no clock pulse. When both S and R are grounded, both outputs Q and $\overline{Q}$ are in the 1–state. The subsequent state of the output will depend upon which ground is released first.

## a typical application of the WM 213 synchronous decade counter

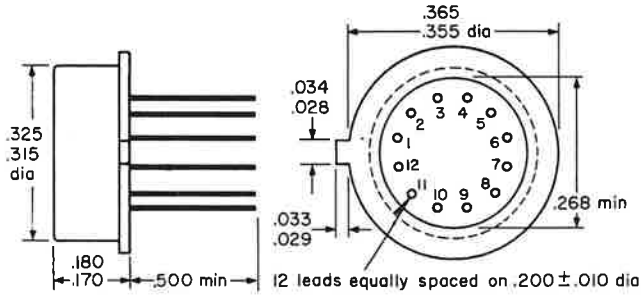



The logic diagram accomplishes the function specified in the truth table. The system is a clocked decimal counter stage.

| D | C | B | A | DECIMAL NUMBER |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |

## mechanical characteristics

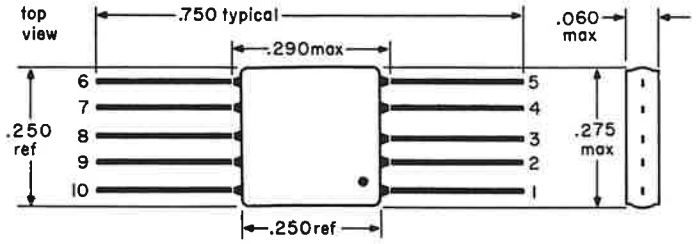
### T package—12 pins • 1.1 grams (typical)




PIN NUMBERING

1. Output, Q
2. Node, $R_N$
3. DC Reset, R
4. + $V_{CC}$
5. D.C. Set, S
6. Node, $S_N$
7. Output, $\overline{Q}$
8. Clocked Reset, $R\overline{Q}$
9. Clock, C
10. Ground
11. Open
12. Clocked Set, SQ

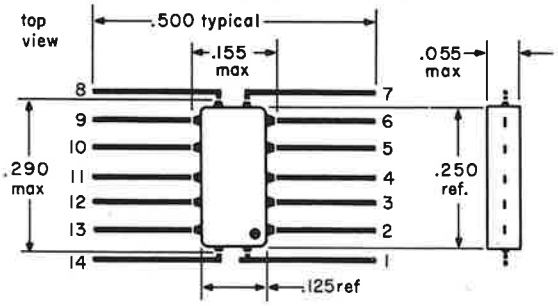
### Q style FLAT-PAK • 0.25 grams (typical)




Gold plated Kovar® leads are 15 x 5 mils on 50 mil centers.

1. Clock, C
2. Clocked Set, SQ
3. Output, Q
4. Node, $R_N$
5. D.C. Reset, R
6. + $V_{CC}$
7. D.C. Set, S
8. Output, $\overline{Q}$
9. Clocked Reset, $R\overline{Q}$
10. Ground

### G style FLAT-PAK • 0.1 grams (typical)




Gold plated Kovar leads are 12 x 4 mils on 50 mil centers.

1. Clock, C
2. Clocked Set, SQ
3. Output, Q
4. Ground ★
5. Node, $R_N$
6. D.C. Reset, R
7. + $V_{CC}$
8. Open
9. D.C. Set, S
10. Node, $S_N$
11. Open
12. Output, $\overline{Q}$
13. Clocked Reset, $R\overline{Q}$
14. Ground ★

*Use only pin 14 for circuit ground—
Pin 4 is an internal ground.